SILICON NANOWIRE FIELD EFFECT TRANSISTOR AND CURRENT-VOLTAGE CHARACTERISTICS OF THE DEVICE

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Abstract. Nanowire Field Effect Transistors (NW-FETs) have been one of the most exciting research topics, attracting special attention from scientists worldwide. Many recent studies demonstrate that these devices exhibit excellent electromechanical properties and can be used for manufacturing the next-generation integrated circuits (ICs). This paper presents a model of an NW-FET, consisting of a silicon nanowire placed in the channel to enhance conduction efficiency and mitigate the short-channel effects. A novel approach in this research involves the utilization of the Schrödinger-Poisson equation and the Non-equilibrium Green's Function (NEGF) method to calculate current-voltage characteristics in the component. Subsequently, the calculated results are simulated using Matlab software with various parameters such as channel length, semiconductor doping concentration, and gate oxide thickness, etc. The experiments indicate that the proposed method gives us accurate results and can be applied to other nanoscale devices.

***Keywords*:** Silicon Nanowire Field Effect Transistor, SiNW-FET, Non-equilibrium Green's function, Nanowire devices.

1. INTRODUCTION

In recent years, classical planar Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have reached its scaling limits. Many new designs have been researched to replace the existing planar technology. The success of the 22nm FinFET with a 3D gate structure has opened a new development direction. However, physical limitations such as short-channel effects (SCEs) and self-heating have posed challenges in scaling devices below 10 nm. To address these issues, scientists have focused on nanoelectronics technology over the past few years. Many new nanoelectronic materials have been researched, such as carbon nanotubes (CNT), graphene, quantum dots (QD) and nanowires [1-4], etc. Among these, nanowire is a potential material that can be applied for fabricating Nanowire Field Effect Transistors (NW-FETs), which are basic elements for building blocks of nanoscale integrated circuits. Recently, many studies on this component have been published, revealing numerous interesting properties. For example, the memory structure of Silicon nanowire transistors generated by weak impact ionization, as proposed by Doohyeok Lim et al., indicates that a memory element consisting of two SiNW-FETs operates at high switching speeds and is compatible with CMOS fabrication processes [5]. Moreover, research on Silicon nanowire growth on carbon cloth for flexible Li-ion battery anodes was introduced by Dylan Storan et al., revealing high area charge and discharge capacities (>2 mAh/cm^2) and stable long-term cycling with 80% capacity retention after 200 cycles [6]. Particularly, SiNW-FETs are also used for making medical biosensors for virus testing kits developed by Zhu Shu et al., [7]. These research projects demonstrate that SiNW-FETs exhibit outstanding properties, including excellent conductivity, small size, high-speed switching, and low energy consumption. Unlike traditional transistors, SiNW-FETs leverage the unique properties of nanowires to enhance performance and efficiency. Additionally, they can overcome the disadvantages caused by short-channel effects (SCEs) and leakage current in classical MOSFETs. This breakthrough enables the creation of ultra-compact electronic components and other applications where high precision is essential. Consequently, SiNW-FETs are considered as promising candidates for fabricating nanoscale devices.

2. MATERIALS AND METHODS

2.1. Nanowire meterials

A nanowire is a nanoelectronic material studied since its experimental discovery in the early 1980s [8]. It is a type of nanomaterial in the form of a wire with quasi one-dimensional (1D) structures. Its diameter is about 10 - 20 nm, and the length-to-width ratio is greater than 1000 [9]. A nanowire is considered the smallest element for efficient transport of electrons and excitons. In this structure, quantum mechanical effects are very important. Therefore, it is also called a quantum wire. Nanowires can be prepared from many different materials, such as metals (Ni, Pt, Au, Ag), semiconductors (SiNWs, InP, GaN), insulators (SiO_2, TiO_2), or organic molecules (DNA) [9,10], etc. The image of a typical semiconductor nanowire illustrating its structure and characteristics is shown in Fig.1.

Although many different types of nanowires have been investigated, silicon nanowires are considered popular nanomaterials due to their special electrical and mechanical properties, and they can be readily produced from a silicon precursor by etching of a solid or through catalyzed growth from a vapor or liquid phase [11]. The initial synthesis of SiNWs is often accompanied by thermal oxidation steps to yield structures of accurately tailored size and morphology. For this reason, silicon nanowires can be used for the next generation of field-effect transistors.

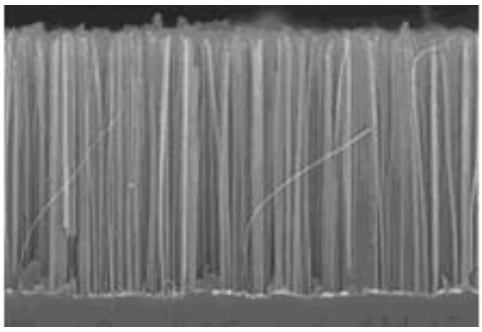

Fig. 1: Cross section of the Silicon Nanowires [12]

The properties of nanowires are similar to the "particle in a box" model, where the size of nanomaterials is smaller than the de Broglie wavelength. Electrons and holes are spatially confined, and electric dipoles are formed, leading to an increase in energy separation between adjacent levels [9], [12, 13]. Additionally, the electron density of states (DOS) dramatically depends on the size of nanostructures [14]. Due to these properties, SiNW has been considered one of the promising candidates for creating nano-scale devices.

With a one-dimensional (1-D) structure, electrons in nanowires are confined in two dimensions. This implies that the electrons are constrained in the radial direction and move freely along the axis of the nanowires. It is assumed that the nanowires have infinite length and act as an infinite 2-D potential well in the radial direction. Thus, the transport in the device is considered to be purely ballistic [15, 16]. The Schrödinger equation describes the band structure, and the energy levels are represented by:

$$H\psi = E\psi \tag{1}$$

Where ψ is the wave function, m is the mass of the particle, E is the total energy, $\hbar$ is the reduced Planck constant, and H is the Hamiltonian operator.

$$H = \left[-\frac{\hbar^2}{2m}\nabla^2 + V \right]$$

By using the Laplace operator for the cylindrical coordinate structure of the nanowire *(r, θ, z)*, equation (1) can be expressed as:

$$\nabla^2_{r,\theta,z} = \frac{\partial^2}{\partial r^2} + \frac{1}{r}\frac{\partial}{\partial r} + \frac{1}{r^2}\frac{\partial^2}{\partial \theta^2} + \frac{\partial^2}{\partial z^2}$$

$$\left[-\frac{\hbar^2}{2m}\left(\nabla^2_{r,\theta,z}\right) + V(r,\theta) \right]\psi(r,\theta,z) = E\psi(r,\theta,z) \tag{2}$$

The equation (2) represents a cylindrical system where the potential is independent of the position along the wire axis (z-axis). It is assumed that the solutions in separable products are represented in equation (3). Therefore, the plane wave solution in the z direction can be ignored, and equation (2) can be rewritten as equation (4).

$$\psi(r,\theta,z) = u(r)\Theta(\theta)e^{ik_z z} \tag{3}$$

$$\nabla^2_{r,\theta} = \frac{\partial^2}{\partial r^2} + \frac{1}{r}\frac{\partial}{\partial r} + \frac{1}{r^2}\frac{\partial^2}{\partial \theta^2}$$

$$\left[-\frac{\hbar^2}{2m}\left(\nabla^2_{r,\theta}\right) + V(r,\theta)\right]\psi(r,\theta) = \varepsilon\psi(r,\theta) \tag{4}$$

Where $\varepsilon = E - \frac{\hbar^2 k_z^2}{2m}$ (5)

The equation (4) represents a 2-D potential well with polar coordinates of radius R. In this case, when R = 0, the potential inside the well is 0, and when R > 0, the potential outside the well is infinite.

At the boundaries of the well, the wave functions are equal to zero, $\psi(r = R,\theta) = 0$. The term θ in equation (4) is a solution to the radial part in equation (3). Where l is limited by the integers, $l = 0, \pm 1, \pm 2\ldots$ The equation (4) is reduced to a radial part inside the well, as in equation (6), which is treated as Bessel's equation:

$$r^2\frac{d^2u}{dr^2} + r\frac{du}{dr} + \left[(kr)^2 - l^2\right]u = 0\,. \tag{6}$$

Where $k = \left(2m\varepsilon/\hbar\right)^{1/2}$, the solutions of Equation (10) are the non-elementary Bessel functions J_l and Y_l. The eigenvalues of the Bessel eigenfunctions are the square of the roots of the corresponding Bessel function with quantum number l. The Bessel function has some roots with eigenvalues $\alpha^2_{i,n}$, where n is the n:th positive root determined from the origin. The wave functions in equation (4) can be re-written as follows:

$$\psi(r,\theta) = J_l\left(\frac{\alpha_{l,n}r}{R}\right)e^{il\theta} \tag{7}$$

$$\varepsilon_{l,n} = \frac{\hbar^2\alpha^2_{l,n}}{2mR^2} \tag{8}$$

The total energy (E) in the system along the z-axis is determined by combining equation (5) and (7), and the sub bands in the conduction band are:

$$E_{l,n}(k_z) = \varepsilon_{l,n} + \frac{\hbar^2 k_z^2}{2mR} \tag{9}$$

By using the Heaviside Step function, the 1-D density of states as a function of the energy for a quantum wire can be represented by equation (10) and the graph of the density of states of the nanowire is shown in Fig.2.

$$n_{1D}(E) = \sum_{l,n}\frac{1}{\pi\hbar}\sqrt{\frac{2m}{E - E_{l,n}}}\Theta\left(E - E_{l,n}\right) \tag{10}$$

Where m is the effective mass, $E_{l,n}$ are the energy eigenvalues from equation (9), Θ is the Heaviside Step function.

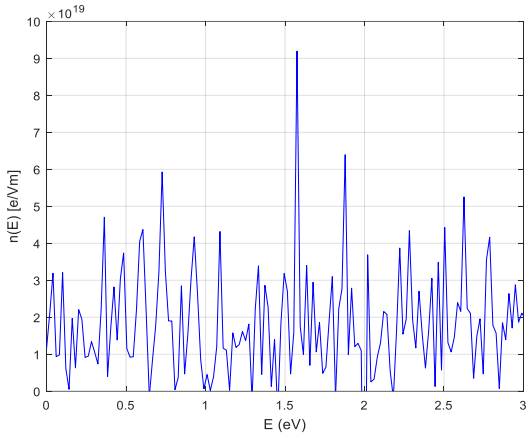

Fig. 2: Density of states of a GaAs Silicon nanowire

2.2. SiNW-FET Model

The introduction of the 22 nm Fin-FET with a 3D gate structure has successfully improved transistor performancetransistor performance and significantly increasing the packing density of microchips. However, further scaling down will cause disadvantages to the performance due to the short channel effects arising from weakened gate control [17]. To solve this problem, one possible solution is to increase the gate capacitance by maximizing the contact surface area between the gate and the channel. This means that the gate oxide thickness must be reduced [18]. However, if the gate oxide becomes too thin, current leakage will occur, increasing power consumption in the off state and reducing reliability.

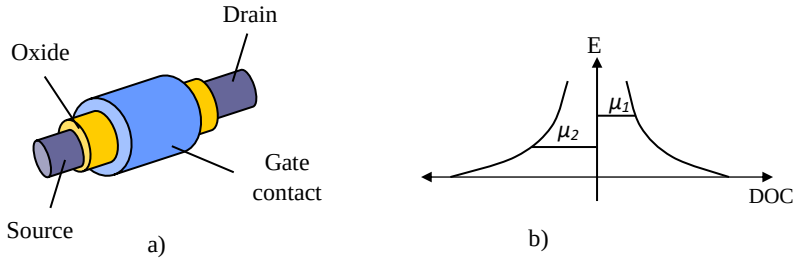

Fig. 3: a) Model of SiNW-FET; b) The Nanowire transverse band diagram

Therefore, a SiNW-FET with the gate all around (GAA) structure is the best solution for scaling devices which can eliminate the disadvantages as mentioned above [19],[20]. As shown in Fig.3, the component consists of three electrodes: gate (G), source (S) and drain (D). Especially, a nanowire is used as a channel to enhance the efficiency of the electrical conduction. The gate electrode is insulated from the channel by a thin oxide layer (SiO_2) taken to be about 1 nm. The source and drain regions are doped by n-type impurity semiconductor with a concentration of $2.10^{20}/cm^3$. The source and drain extension region is approximately 4nm. The channel length is taken to be 5nm and the body thickness (diameter) can be controlled down to well below 5nm. The transport direction is taken to be [100], which is the "x" direction in the device coordinate system, and the confinement directions are [100].

At the equilibrium ($V_{ds} = 0$) the two Fermi energy levels at the source and drain are approximately equal ($\mu_1 = \mu_2$). Therefore, there is no drain-source current in the channel. As the drain voltage is supplied, the two Fermi energy levels will be different ($\mu_1 \neq \mu_2$), and the channel is in a non-equilibrium state. In this case, source and drain Fermi distribution functions are presented by:

$$f_1(E) = \frac{1}{e^{[(E-\mu_1)/k_BT} + 1} = f_0(E - \mu_1) \qquad (11)$$

$$f_2(E) = \frac{1}{e^{[(E-\mu_2)/k_BT} + 1} = f_0(E - \mu_2) \quad (12)$$

Where E is the energy, k_B is the Boltzman's constant (k = 1,38066.10^{-23} J/K), and T is the temperature at 300^0 K. At that time, if the gate voltage is applied ($V_{gs} \neq 0$), an electric field will appear in the channel, leading to current flow from the drain to the source.

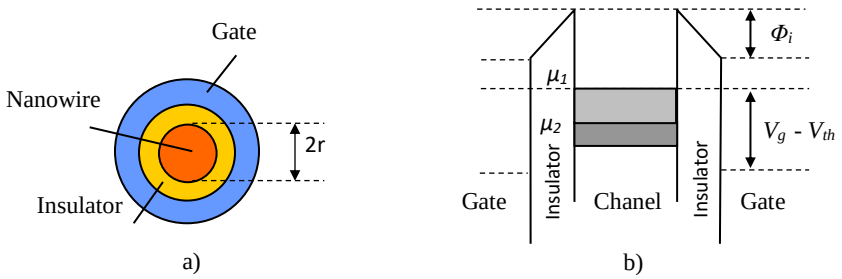

Fig. 4: a) Cross section of SiNW-FET structure; b) The energy band gap of nanowire contact

The work-function (Φ_{MS}) difference between the gate electrode and the semiconductor is defined by:

$$\Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - \chi - \frac{E_g}{2q} - \phi_t \ln\left(\frac{N_{sub}}{n_i}\right) \quad (13)$$

Where, E_g is the semiconductor energy gap, χ the electron affinity ($q\chi = E_v - E_c$), q is the electron charge, ϕ_t is the thermal potential, N_{sub} is the substrate doping concentration, and n_i is the intrinsic doping concentration (n ≈ 10^{10} cm^{-3} at T = 300^0 K).

The thermal potential is $\phi_t = \ln\frac{kT}{q}$; the bulk potential is $\phi_F = \phi_t \ln\left(\frac{N_A}{n_i}\right)$.

In the SiNW-FET, the equation stands for the threshold voltage depends on the work function [21], radius of device, thickness of oxide and the permittivity of oxide and material that is represented by:

$$V_{th} = \Delta\Phi + \frac{kT}{q}\ln\left(\frac{8kT\varepsilon_s}{q^2 n_i}\right) - \frac{2kT}{q}\ln\left(\frac{1+t_{ox}}{R}\right)^{\frac{2\varepsilon_s}{\varepsilon_{ox}}} \quad (14)$$

Where $\Delta\Phi$ is the work function difference, R is the radius of the device, k is Boltzmann's constant, T is temperature, n_i is the intrinsic doping parameter for the substrate, and q is the charge of an electron.

2.3. Non-Equilibrium Green's Function

Non-equilibrium Green's function (NEGF) method is regularly used to calculate current and charge densities in nanoscale devices. This method is mainly applied in ballistic conduction and inelastic scattering. In the SiNW-FET structure, there are differences between the two Fermi levels of the drain and source. Thus, we can use the NEGF method to describe the parameters of the component [22, 23. The NEGF model is represented in Fig.5a, where the Hamiltonian operator is used to describe the channel properties; μ_1 is the Fermi levels at the source, and μ_2 is the Fermi levels at the drain contacts. The effects of the source and drain contacts are described by the self-energy matrices Σ_1 and Σ_2, respectively.

As the electrons move to the channel, the contact voltage will increase, causing a change in the electron density in the channel. This process continues until the contact voltage reaches a steady state (self-consistent). The Non-equilibrium Green's function at the energy level E is given by:

$$G(E) = \left[\left(E + i0^{+}\right)I - H - U_{SC}\right]^{-1} \quad (15)$$

Where I is the unit matrix; H is the Hamiltonian operator, U_{SC} is the self – consistent voltage.

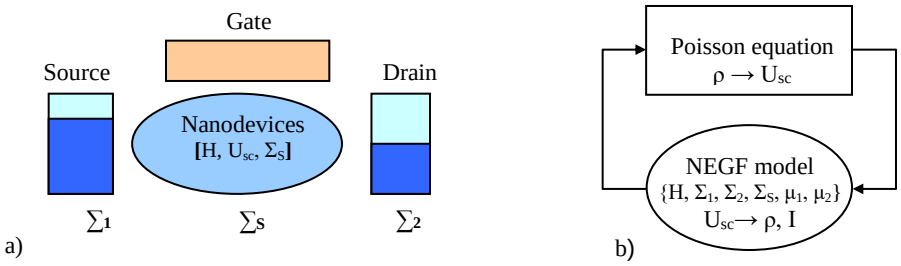

Fig. 5: a) The NEGF model; b) The relation parameters between NEGF and Poisson function

Under the influence of an electric field, electrons moving from the source to the drain can collide with each other. As a result, some of their energy is exchanged, a phenomenon described by ballistic and phonon scattering transport. Therefore, the Non-equilibrium Green's function is fully rewritten as:

$$G(E) = \left[\left(E + i0^{+}\right)I - H - U_{SC} - \sum_1 - \sum_2\right]^{-1} \quad (16)$$

Where Σ_1 and Σ_2 are the self-energies of the source and drain, respectively, which are considered to be the boundary conditions of the Schrodinger-Poisson equation.

In the silicon nanowire, the movement of electrons is close to the form of ballistic transport. Thus, the Non-equilibrium Green's functions in this case can be:

$$G(E) = \left[\left(E + i0^{+}\right)I - H - \sum_1 - \sum_2\right]^{-1} \quad (17)$$

The density matrix is then calculated from the correlation function:

$$\rho = \frac{1}{2\pi}\int [-iG^{"}(E)]dE \quad (18)$$

Where - *iG''(E)* is the correlation function, and it can be determined from the Greens Function as:

$$-iG^{"}(E) = G(f_1\Gamma_1 + f_2\Gamma_2)G^{+} \quad (19)$$

The interaction of energy at the drain and the source is calculated by the Gamma function as:

$$\Gamma_{1,2} = i\left(\sum_{1,2} - \sum_{1,2}^{+}\right) \quad (20)$$

The electron density $n(\vec{r})$ in real space is calculated by:

$$n(\vec{r}) = \sum_{\alpha,\beta}\Psi_{\alpha}(\vec{r})\Psi_{\beta}(\vec{r})\rho_{\alpha,\beta} \quad (21)$$

The Poisson equation represents for the change in electron density in the channel:

$$\vec{\nabla}\left[\varepsilon\vec{\nabla}U(\vec{r})\right] = -q^2\left[n(\vec{r}) - n_0(\vec{r})\right] \quad (22)$$

Where the self-consistent $U_{SC} = UI$; I is the unit matrix.

The total number of electrons N can be calculated from the density matrix as follows

$$N = Trace(\rho) \quad (23)$$

When the self-consistency is reached, the transmission probability *T(E)* is calculated by the relation:

$$T(E) = Trace(\Gamma_1 G\Gamma_2 G^{+}) \quad (24)$$

The drain current (I_{ds}) flowing in the device is calculated by the Landauer–Büttiker formula as follows [24]:

$$I_{ds} = \frac{2q}{h}\int_{-\infty}^{+\infty} T(E)\left[f_1(E) - f_2(E)\right]dE \quad (25)$$

Where h is the Planck constant, and q is the electric charge.

3. RESULTS AND DISCUSSION

As presented in section 2.2, the SiNW-FET structure with the gate-all-around circular (GAA) configuration has been thoroughly analyzed. In this section, we used Matlab software to simulate the current-voltage characteristics for various parameters such as channel length variation, doping concentration in the semiconductor wafer, gate oxide thickness, and nanowire sizes, etc. The standard values used in simulations are based on the 10nm technology node [19], as shown in Table 1.

Table 1. The parameters used in simulating the SiNW-FET.

Parameters	Descriptions	Standard values used in simulations
L, W	Channel length and channel width	10 nm
ε	Effective dielectric constant	8
ε_{ox}	Dielectric constant of insulator	3.9
T_{si}	Silicon body thickness	10 nm
N_A	P^+ Source doping	$10^{20}/cm^3$
N_D	N^+ Drain doping	$10^{20}/cm^3$
T_{ox}	Thickness of insulator layer (SiO_2)	1 nm
C_{ox}	Capacitance of insulator	11.10^{-6} C/cm^2
C_{nw}	Capacitance of NW gate	2.10^{-7} C/cm^2
V_{gs}	Gate-source voltage	0.8 V
V_{ds}	Drain-source voltage	0.8 V

Similar to the transfer characteristic in classical planar MOSFETs, the drain-source current (I_{ds}) of the SiNW-FET is controlled by both the drain-source voltage (V_{ds}) and gate voltage (V_{gs}). As shown in Fig. 6a, when V_{gs} is held constant at 0.8V, if the drain voltage is less than the threshold voltage, I_{ds} will increase exponentially. Once the drain voltage exceeds the threshold voltage, I_{ds} will remain almost unchanged (in the saturation state). Similarly, when V_{ds} is fixed at 0.8V, as V_{gs} increases from 0.2V, 0.4V, 0.6V to 0.8V, I_{ds} gradually rises, reaching saturation current at 0.16μA, 0.32μA, 0.53μA, and 0.78μA, respectively. However, in SiNW-FET, the threshold voltage changes with the variation of gate voltage. Fig.6b shows that as the drain-source voltage varies from 0.1V to 0.8V, the threshold voltage increases from 0.074V to 0.103V, respectively.

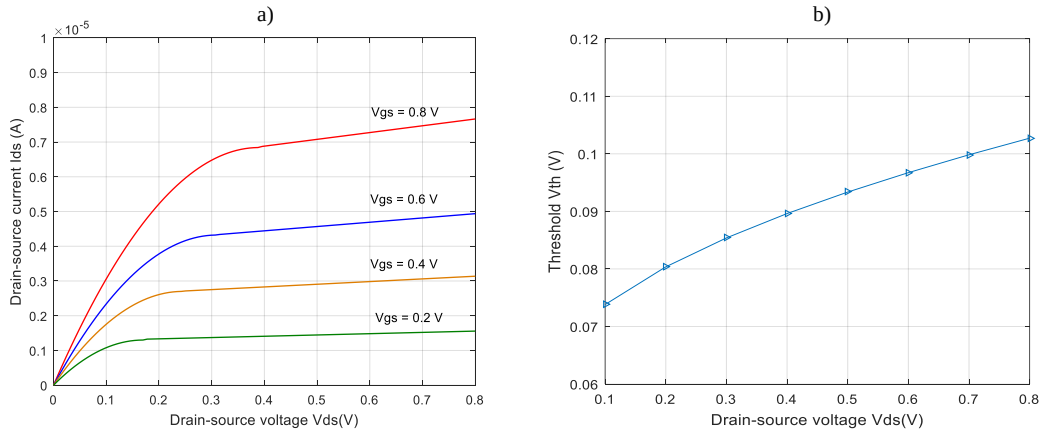

Fig. 6: a) Plot of I_{ds}-V_{ds} by varying the different gate voltages V_{gs}; b) Plot of variou threshold voltage as a function of the drain-source voltage

Fig.7a represents the I_{ds} - V_{gs} characteristics with various oxide thicknesses (T_{ox}). It shows that as the dielectric thickness decreases, the drain-source current increases significantly, reaching a maximum at the smallest oxide thicknesses. At a gate voltage of 0V, for oxide thicknesses of 1nm, 2nm, 3nm, and 4nm, the I_{ds} current is approximately 0.672μA, 0.465μA, 0.286μA, and 0.102μA respectively. However, if the oxide layer is too thin,

leakage current may occur, leading to the possibility of the oxide layer being punctured as the gate voltage increases. Fig.7b shows the relationship between the threshold voltage (V_{th}) and the oxide thickness. It indicates that as the oxide thickness increase, the threshold voltage exhibits a downward trend. Thus, the variation in threshold voltage is a function of the gate oxide thickness.

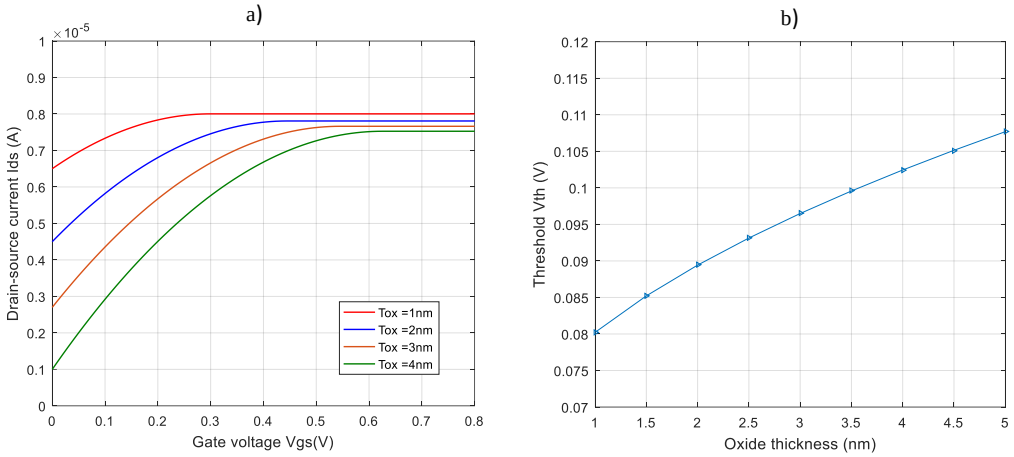

Fig. 7: a) The I_{ds}-V_{gs} characteristics of SiNW-FET with various oxide thickness
b) Plot of various threshold voltages as a function of the gate length

Fig.8a illustrates the dependence of drain-source current (I_{ds}) on different semiconductor doping concentrations (N_{sub}). One major requirement for transistor design is the ability to control carrier concentration. As the doping concentration in the source and drain increases, the barrier becomes slightly higher due to shift in the Fermi level, but also thinner, leading to a decrease in thermionic emission as well as an increase in drain-source current. At a gate voltage of 0V, for the doping concentrations $N_1 = 10^{23}cm^{-3}$, $N_2 = 10^{22}cm^{-3}$, $N_3 = 10^{21}cm^{-3}$, and $N_4 = 10^{20}cm^{-3}$, the drain-source current is approximately 0.56μA, 0.401μA, 0.262μA, and 0.102μA, respectively. However, semiconductor doping concentration also depends on microelectronic fabrication technology. In current research, N_{sub} ranges from about $10^{16}cm^{-3}$ to $10^{23}cm^{-3}$. Fig.8b shows the relationship between the threshold voltage and semiconductor doping concentration. It demonstrates that as semiconductor doping concentration rises, the threshold voltage also exhibits an upward trend. Thus, the variation in threshold voltage is a function of semiconductor doping concentration.

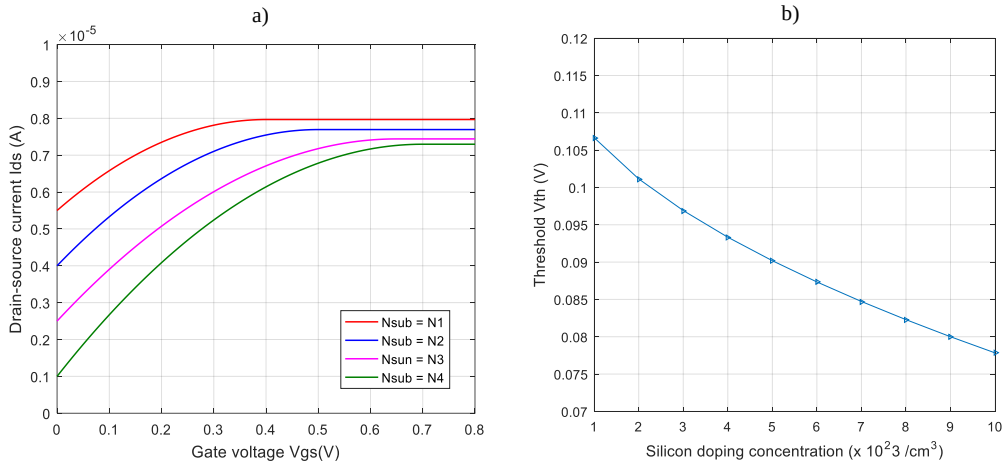

Fig. 8: a) Plot of I_{ds}-V_{gs} characteristics with various doping profile, where $N_1 = 10^{23}$ cm^{-3}, $N_2 = 10^{22}$ cm^{-3}, $N_3 = 10^{21}$ cm^{-3}, $N_4 = 10^{20}$ cm^{-3} ; b) Plot of various threshold voltages as a function of source and drain doping concentration

Fig.9a represents the relationship between the drain-source current (I_{ds}) and gate voltage (V_{gs}) by varying the silicon nanowire channel length (L_{ch}). It shows that as L_{ch} increases, I_{ds} decreases. For channel lenghs going up from L=10nm, 12nm 14nm to 15nm, the drain-source current is found to be 5.321µA, 4.035µA, 2.625µA and 1.102µA respectively. Obviously, the variation of I_{ds} is nonlinear with the change of nanowire sizes. Fig.9b shows the variation of threshold voltage by varying the channel length. The more the channel length increases, the more the threshold voltage goes up. In classic planar MOSFET, the threshold voltage remains almost constant. However, in SiNW-FET, the threshold voltage always changes depending on the device parameters, which is a different from other nanoelectronic devices.

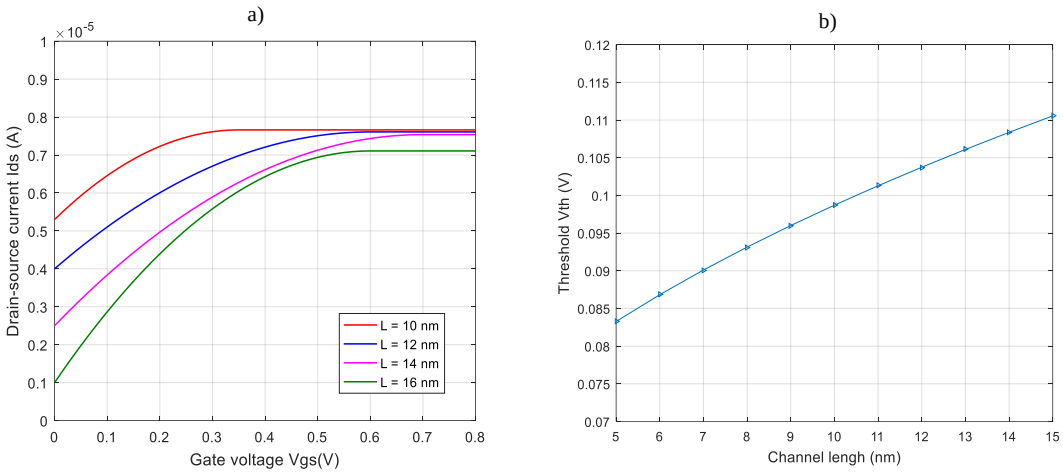

Fig. 9: a) Plot of I_{ds} -V_{gs} by varying the different channel length L_{ch}; b) Variation of threshold voltage as a function of channel length.

4. CONCLUSION

Simulating the performance of a new device is a crucial step in the integrated circuits manufacturing process, significantly reducing time and costs for design and fabrication. The study results indicate that the drain current depends not only on the gate voltage but also on material parameters such as channel length, gate oxide thickness, and doping concentration in the semiconductor, etc. In particular, the threshold voltage also varies depending on changes in these parameters. Thus, the NW-FET holds promise for future innovations in quantum computing, as its nanoscale dimensions align with the requirements of quantum bits. This intersection of nanotechnology and quantum computing opens up new possibilities for faster, more powerful, and energy-efficient electronic systems. As research continues to unfold, the SiNW-FET stands as a testament to the remarkable strides being made in the realm of nanoelectronics. However, the SiNW-FET is still in the research phase, and many device parameters need to be analyzed more carefully. Consequently, the above research results have contributed to clarifying the outstanding characteristics of this special device.

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TRANSISTOR HIỆU ỨNG TRƯỜNG DÂY NANO SILICON VÀ ĐẶC TRƯNG DÒNG ĐIỆN – ĐIỆN THẾ CỦA LINH KIỆN

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Tóm tắt. Transistor hiệu ứng trường dây Nano Silicon (NW-FET) là một trong những chủ đề nghiên cứu hấp dẫn nhất, thu hút sự quan tâm đặc biệt của các nhà khoa học trên toàn thế giới. Nhiều nghiên cứu gần đây chứng minh rằng linh kiện này thể hiện các đặc tính cơ - điện tuyệt vời và có thể được áp dụng để chế tạo các vi mạch tích hợp (ICs) thế hệ tiếp theo. Bài viết này trình bày một mô hình SiNW-FET, bao gồm một dây Nano Silicon được đặt trong kênh dẫn để tăng cường hiệu quả hoạt động và giảm thiểu hiệu ứng kênh ngắn. Một hướng tiếp cận mới trong nghiên cứu này là sử dụng phương trình Schrödinger-Poisson và phương pháp Hàm Green không cân bằng (NEGF) để tính toán các đặc trưng dòng điện-điện thế trong linh kiện. Sau đó, các kết quả tính toán được mô phỏng bằng phần mềm Matlab với các thông số khác nhau như độ dài kênh, nồng độ pha tạp chất bán dẫn, độ dày oxit cổng...Những kết quả thực nghiệm cho thấy rằng phương pháp đề xuất cho kết quả tính toán chính xác và có thể áp dụng cho các linh kiện điện tử nano khác.

Từ khóa: Transistor Hiệu ứng Trường dây Nano, SiNW-FET, Hàm Green không Cân bằng, Linh kiện Nanowire.

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