ANALYSIS THE EFFECTS OF FERROELECTRIC ELECTRIC FIELD ON CURRENT-VOLTAGE CHARACTERISTICS OF THE FERROELECTRIC FIELD EFFECT TRANSISTOR USING $SRBI_2TA_2O_9$ THIN FILM

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Abstract. This paper presents a new analytical expression for current-voltage characteristics of the Ferroelectric Field Effect Transistor (FeFET), a promising candidate for nonvolatile memories. For this research, a FeFET model using Pt/$SrBi_2Ta_2O_9$/Insulators/Si thin film as an effect gate stack was proposed and assessed. Firstly, we have studied the effects of ferroelectric polarization on current-voltage characteristics of FeFET based on the analytical method of CMOS device, the polarization hysteresis properties versus electric field (P-E) of the ferroelectric material was explicitly analysed with two parameters of saturated and unsaturated polarization. Then, by mathematical analysis, the current-voltage values was calculated under different conditions such as using differences of substrate doping concentration, oxide thickness, ferroelectric thickness, working temperature, etc. Finally, the calculated results were simulated by the Matlab software that gave us an overview of the device properties.
Keyworks. *Ferroelectric, Ferroelectric Field Effect Transistor, FeFET, nonvolatile memory*.

1. INTRODUCTION

In recent years, Ferroelectric Field Effect Transistor has been intensively researched for use in nonvolatile memory devices, in particular, ferroelectric random access memories (FRAM). As a nonvolatile memory element, FeFET have many advantages in high-density integration, low power dissipation, non-destructive readout operation, and good scalability [1]. A variety of FeFET had been investigated over the past time [2-3] interested by many research groups. However, despite much effort by a lot of researchers, data retention time of FeFET has been in short. The reasons for these were the effects of depolarization field [4] and unsaturated polarizations in ferroelectric layers [5] have been discussed. Many methods to improve have been proposed such as ferroelectric capacitors have been successfully integrated with silicon electronics, where the polarization state was read out by a device based on a field effect transistor configuration (MFIS) and a good process for FeFET having long data retention [6-8]. Since then, FeFET became a promising candidate in the application for nonvolatile memories. In this paper, we continuously investigated the FeFET using method of mathematical calculation to analysis spontaneous polarization components in ferroelectric material and study the effects of ferroelectric polarization on current-voltage characteristics of the device.

2. FERROELECTRIC MATERIALS AND FEFET MODEL

2.1. Ferroelectric materials

Ferroelectric is a special material which has its own spontaneous electric polarization at a certain temperature range and that spontaneous electric polarization can be altered by the external electric field. The first ferroelectric material was found in the Rochelle NaK salt ($C_4H_4O_6$) $4H_2O$ since 1920. Because of the electrical properties of Rochelle salts similar to the magnetic properties of ferromagnetic materials, the term "ferroelectric material" derives from thence.

According to E. Nakamura and T. Mitsui [9], there exist more than 600 different types of ferroelectric and anti-ferroelectric materials. Ferroelectric materials can be divided into three different groups: The first are hydrogen-bonded systems like KDP, the second are ionic crystals with perovskite-type such as Barium Tinanat that are the most widely used and the third are narrow semiconductors like

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GeTe, many exhibit ferroelectric properties. In which, the two most widely used ferroelectric materials are $Pb(Zr,Ti)O_3$ of the PZT group and $SrBi_2Ta_2O_9$ of the SBT group.

Strontium Bismuth Tantalate ($SrBi_2Ta_2O_9$) is the most important ferroelectric material in the application for nonvolatile memories. It was discovered by Smolenskii et al in 1961. Its attributes are low fatigue, low coercive field and Pb-free compound [10]. At the room temperature, $SrBi_2Ta_2O_9$ is orthorhombic, the space group is $A2_1am$ (C_{2v}^{12}, number 36 in the standard listing). The dimensions of the rectangular parallelepiped unit cell are (in Å) a = 5.531, b = 5.534, c = 25.984. This unit cell contains four $SrBi_2Ta_2O_9$ formula units (56 atoms). The primitive cell (the smallest translational unit) is containing two formula units (28 atoms). Its crystal consists of perovskite-type $(SrTa_2O_7)^{2-}$ groups (two layers of TaO_6 octahedra) and semiconductor $(Bi_2O_2)^{2+}$ layers. It undergoes two phase transitions at 608 K (T_C) and 850 K (T_H). The spontaneous polarization is large about $P_s \approx 5.8$ - 10 μC/cm^2 along the a-axis at room temperature. The high temperature paraelectric phase is tetragonal with space group I4/mmm (a = 3.927, and c = 25.142 Å at 1000 K), where the TaO_6 octahedra take antiparallel arrangements along the tetragonal c-axis as show in Fig. 1a [12].

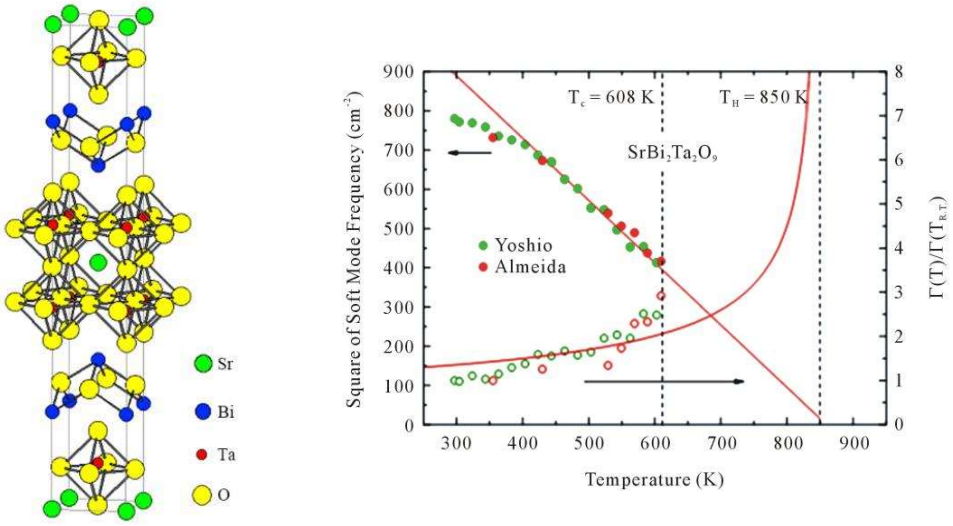

Fig.1. a) Crystal structure Bi-layered perovskite $SrBi_2Ta_2O_9$,;
b) The phase transitions of $SrBi_2Ta_2O_9$ are observed at T_C = 608 K and T_H = 850 K. [11]

2.2. FeFET model and Ferroelectric polarization

FeFET is a type of field effect transistor, consisting of three electrodes as gate G, source S and drain D shown in Fig. 2, its working principle based on the electric field effect similar to a MOSFET. In gate stack of the FeFET, a thin ferroelectric layer was placed on the oxide layer to create an effect gate stack that can be saved the nonvolatile polarization to operate even the gate voltage is no longer. Thus, operation of the device is as a memory element. Because of remnant polarization of ferroelectric in the stack gate, the working principle of FeFET was described as the combination of the MOSFET and the ferroelectric capacitor.

According to experimented data of T. Kanashima et al [13], the surface charge of the ferroelectric on per unit area consists of linear polarization and nonlinear polarization component because of its ferroelectric effects.

$$Q_{Fe} = \left(P_{nonlin} + P_{lin}\right).A = \left(P_{nonlin} + \varepsilon_o \varepsilon_r E\right).A \quad (1)$$

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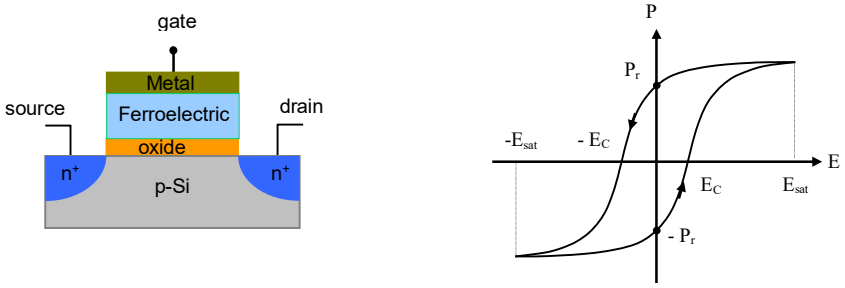

Fig. 2. a) FeFET model, b) *Ferroelectric* polarization hysteresis loop

Where $A = L.W$ (L and W are length and width of channel, respectively), ε_F is the dielectric constant of the linear part of the ferroelectric, ε_o is the free space permittivity. The nonlinear saturated *P-E* hysteresis loop was determined by the mathematical model of Miller et al [14].

$$P_{sat}^{+} = P_s \tanh\left(\frac{E_{Fe} - E_C}{2\delta}\right) \tag{2}$$

$$\delta = E_C \ln\left[\left(1+\frac{P_r}{P_s}\right)/\left(1-\frac{P_r}{P_s}\right)\right]^{1/2}$$

$$P_{sat}^{-} = -P_{sat}^{+}(-E_C)$$

Where E_C is the coercive field, P_r is the remnant polarization and P_s is the saturated polarization. The positive sign in the expression for P_{Fe} is for the ascending and the negative for the descending hysteresis branch.

Fig. 3. The FeFET polarization direction is determined by the gate voltage bias.
a) FeFET with a positive gate voltage bias; b) FeFET with a negative gate voltage bias.

However, these equations are only indicated for the saturated polarization state. Thus, the unsaturated polarization state can be determined by a maximum electric field parameter that the ferroelectric layer may undergo, E_m. The unsaturated hysteresis loop is composed of two branches $P^{+}(E)$ and $P^{-}(E)$, where $P^{+}(E)$ is the positive branch and $P^{-}(E)$ is the negative one. These two branches must intersect at $E = E_m$:

$$P^{+}(E_m) = P^{-}(E_m) \tag{3}$$

As Miller and McWhorter indicated [14], the derivative of the polarization with respect to the electric field, where E is constant field, is independent of the amplitude of the applied signal at least to first order

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$$\frac{dP^{+}(E_m)}{dE} = \frac{dP^{+}_{sat}(E)}{dE} \tag{4}$$

and

$$\frac{dP^{-}(E_m)}{dE} = \frac{dP^{-}_{sat}(E)}{dE}$$

From equation (4), the dependence of the dipole polarization on the maximum electric field is determined by [15]:

$$P_d(E_m) = +\varepsilon_F \varepsilon_o E_m + \frac{1}{2}\left[P_s \tanh\left(\frac{E_m + E_c}{2\delta}\right) + P_s \tanh\left(\frac{E_m - E_c}{2\delta}\right)\right] \tag{5}$$

At $E = 0$, ferroelectric material is not polarization ($P = 0$), the polarization will increase when increasing the applied electric field. The polarization will follow the curve of $P_d(E_m)$ until the maximum field E_m.

2.3. Current-voltage characteristic in MFIS-FET

a. MFIS gate stack capacitance

As equation (1), the capacitance of the ferroelectric is determined by:

$$C_{Fe} = \frac{Q_{Fe}}{V_{Fe}} = \frac{(P_{nonlin} + \varepsilon_o \varepsilon_r E).A}{V_{Fe}} = C_{Fe-nl} + C_{Fe-l} \tag{6}$$

Where C_{Fe-l} and C_{Fe-nl} are non-linear capacitance and linear dielectric capacitor, respectively. The linear capacitance is determined by:

$$C_{Fe-l} = \frac{\varepsilon_o \varepsilon_r E}{V_{Fe}} A = \frac{\varepsilon_o \varepsilon_r}{T_{Fe}} A \tag{7}$$

From equation (2), the non-linear capacitance value caused by ferroelectric effect was determined by:

$$C_{Fe-nl} = \pm P_s \tanh\left[\left(\pm\frac{V_{Fe}}{T_{Fe}} - E_C\right)/(2\delta)\right]\frac{A}{V_{Fe}} \tag{8}$$

Where $\delta = E_C \ln\left[\left(1+\frac{P_r}{P_s}\right)/\left(1-\frac{P_r}{P_s}\right)\right]^{1/2}$

From equation (6), the gate stack of MFIS-FET can be modeled as a non-linear ferroelectric capacitor in connecting parallel to a linear ferroelectric capacitor that continuously connected to an oxide capacitor [16] as shown in Fig. 4.

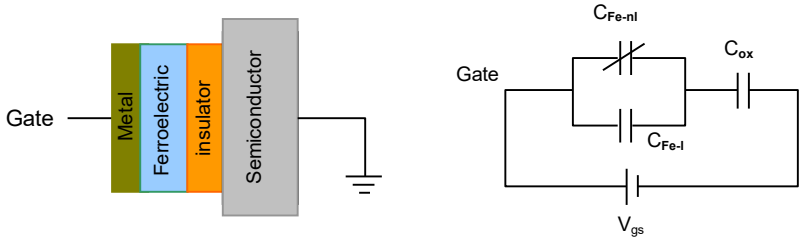

Fig. 4. Ferroelectric capacitors in FeFET gate stack

Therefore, the total capacitance in gate stack is determined as:

$$C_{tt} = \left(\frac{1}{C_{Fe}} + \frac{1}{C_{ox}}\right)^{-1} \tag{9}$$

Where C_{ox} is capacitance of an oxide layer, $C_{ox} = \frac{\varepsilon_o \varepsilon_{ox}}{T_{ox}} A$

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b. Current-voltage characteristic

The energy diagram of MFIS-FET is shown in Fig. 5; the total sum of voltages across the gate stack is determined by [17]

$$V_{gs} = V_{FB} + V_{Fe} + V_{ox} + \phi_s \tag{10}$$

Where ϕ_s is the surface potentials of semiconductor, V_{ox} is the voltage across the oxide, V_{Fe} is the voltage across the ferroelectric layer, V_{FB} is the flat-band voltage.

At $V_{gs} = 0$, the flat-band voltage is given by [18]:

$$V_{FB} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}} \pm \left(\frac{P_{Fe}}{C_{Fe}}\right) \tag{11}$$

Where Φ_{MS} is the work-function difference between the gate electrode and the semiconductor, Q_{ox} is the oxide charge per area, C_{ox} is the oxide capacitance per area, C_{Fe} is the ferroelectric capacitance per area and P_{Fe} is the ferroelectric polarization.

$$\Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - \chi - \frac{E_g}{2q} - \phi_t \ln\left(\frac{N_{SUB}}{n_i}\right) \tag{12}$$

E_g is the semiconductor energy gap, χ the electron affinity ($q.\chi = E_v - E_c$), q the electron charge, ϕ_t the thermal potential, N_{SUB} the substrate doping concentration and n_i the intrinsic doping concentration ($n \approx 10^{10}$ cm^{-3} at T = 300 K).

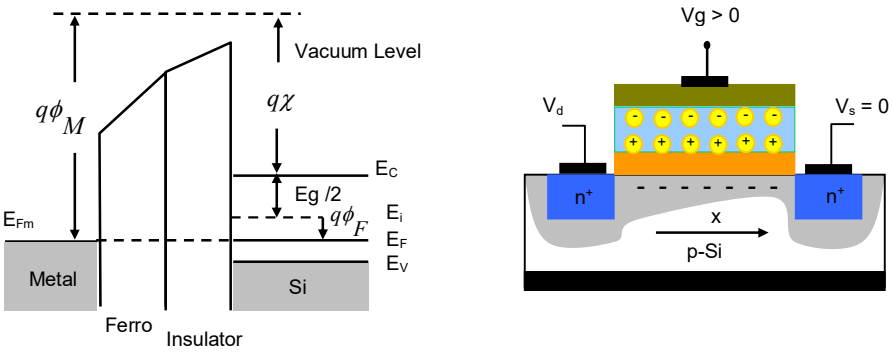

Fig. 5. Energy diagram and electron transportation of MFIS-FET

The thermal potential is $\phi_t = \ln\frac{kT}{q}$, the bulk potential due to doping is $\phi_F = \phi_t \ln\left(\frac{N_A}{n_i}\right)$

In the MFIS structure, the depolarization field in the ferroelectric causes the incomplete charge compensation at the interfaces to the oxide or semiconductor [16]. Thus, that V_{Fe} and V_{ox} are the voltage drop across the ferroelectric and oxide layer is given by:

$$V_{Fe} = \frac{T_{Fe}}{\varepsilon_o \varepsilon_r}(Q_G - P_{Fe}); \quad V_{ox} = \frac{T_{ox}}{\varepsilon_o \varepsilon_{ox}} Q_G \tag{13}$$

The body effect coefficient defined as $\gamma \equiv \frac{\sqrt{2q\varepsilon_o \varepsilon_s N_{SUB}}}{C_{tt}}$

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Basing on Gauss's law, the electric displacement fields of different layers are inter-related as

$$Q_G + Q_{Fe} + Q_{ox} + Q_s = 0 \tag{14}$$

The Q_s are the charge at the gate electrode and inverted channel

$$Q_s = \pm C_{tt}\,\gamma\left[\phi_t e^{-\frac{\phi_s}{\phi_t}} + \phi_s - \phi_t + e^{-\frac{2\phi_F}{\phi_t}}\left(\phi_t e^{-\frac{\phi_s}{\phi_t}} - \phi_s - \phi_t\right)\right]^{1/2} \tag{15}$$

If the charge of oxide player is zero ($Q_{ox} = 0$), then $Q_G = -Q_s$

$$V_{gs} = V_{FB} + \phi_s - \frac{Q_G}{C_{tt}} \tag{16}$$

The gate-source voltage with ferroelectric effect is determined by:

$$V_{gs(Fe)} = V_{gs} + \frac{T_{Fe}}{\varepsilon_o \varepsilon_r} P_{Fe} = V_{FB} + \phi_s + \frac{Q_G}{C_{tt}} \tag{17}$$

From equation (15), the gate-source voltage with ferroelectric effect is rewritten by:

$$V_{gs(Fe)} = V_{FB} + \phi_s \pm \gamma\left[\phi_t e^{-\frac{\phi_s}{\phi_t}} + \phi_s - \phi_t + e^{-\frac{2\phi_F}{\phi_t}}\left(\phi_t e^{-\frac{\phi_s}{\phi_t}} - \phi_s - \phi_t\right)\right]^{1/2} \tag{18}$$

Assuming that electron mobility is constant, μ_n, using the simple charge control model the absolute value of the electron velocity is given by:

$$v_n = \mu_n \frac{dV}{dx} \tag{19}$$

With the gate voltage depend on the threshold voltage V_{TH} and the drain current I_d is given by

$$I_{ds} = Wq\mu_n \frac{dV}{dx} n_s \tag{20}$$

$$dV = \frac{I_{ds}}{W\mu_n C_{tt}\left(V_{gs} - V_{TH} - V_x\right)} dx \tag{21}$$

Where dV versus dx dependence represents a series connection of the elementary parts of FeFET channel

$$\left(V_{gs} - V_{TH} - V_x\right) dV = \frac{I_{ds}}{W\mu_n C_{tt}} dx \tag{22}$$

Similar to the MOSFET, channel resistivity of FeFET is from zero conductivity below threshold voltage to a finite constant conductivity beyond. Integrating along the channel from $x = 0\left(V_x = 0\right)$ to $x = L\left(V_x = V_{ds}\right)$. Based on the calculation in [16], the drain-source current (I_{ds}) can be mathematically determined by:

$$I_{ds} = \frac{W}{L}\mu_n C_{tt}\left(V_{gs} - V_{TH}\right)V_{ds} \text{ for } V_{TH2} < V_{gs} < V_{TH1} \tag{23}$$

and

$$I_{ds} = 0 \text{ for } V_{gs} < V_{TH2} \cap V_{TH2} < V_{gs} < V_{TH1}$$

At strong inversion condition, V_{TH} consists of two states V_{TH1} and V_{TH2} which are determined by [19]

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$$V_{TH1} = V_{FB1} + \frac{1}{C_{F1}}\left[\sqrt{4\varepsilon_s\varepsilon_o\phi_s qN} - P(E_{F1})\right] + V_{ox} + \phi_s \quad (24)$$

$$V_{TH2} = V_{FB2} + \frac{1}{C_{F2}}\left[\sqrt{4\varepsilon_s\varepsilon_o\phi_s qN} - P(E_{F2})\right] + V_{ox} + \phi_s \quad (25)$$

The memory window width is defined by $\Delta T = V_{TH2} - V_{TH1}$. The equation (23) showing that the I_{ds} in FeFET is proportion dependence on the gate stack capacitance, C_{tt}. So, it will also have the same hysteresis characteristics as the ferroelectric polarization.

3. SIMULATION RESULTS AND DISCUSSION

The FeFET model is used in simulation as shown in Fig. 2a. The gate, drain and source electrodes are 50 nm - thick metal (Pt). The buffer oxide layer with high dielectric constant as Al_2O_3 is used. The channel dimension of length and width are changed about 45 nm to 130 nm. The $SrBi_2Ta_2O_9$ thin film is placed on the oxide layer of gate stack. The silicon wafer has the doping concentration of $N_a \geq 10^{16}$ cm^{-3}. The parameter of the component used for simulation is shown in table 1.

Table 1. Parameters used for simulation in the FeFET

Parameter	Description	Values used in simulation
ε_{Fe}	Dielectric constant of ferroelectric	200
ε_{ox}	Dielectric constant of insulator	3.9
E_C	Coercive field	50 kV/cm
P_r	Remnant polarization	10 μC/cm^2
P_s	Spontaneous polarization	15 μC/cm^2
T_{Fe}	Thickness of ferroelectric layer	50 nm
T_{ox}	Thickness of insulator layer	1 nm
μ	Electron mobility	500 cm^2/V.s
N_A	Substrate doping concentration (p-type)	10^{16} cm^{-3}
L	Channel length	45 nm
W	Channel width	45 nm
V_{gs}	Gate-source voltage	1.1 V
V_{ds}	Drain-source voltage	1.1 V
V_{FB}	Flat-band voltage	- 0,5 V

3.1. The polarization hysteresis loop of ferroelectric

As previous discussion, the spontaneous electric polarization of ferroelectric depends on the external electric field, the electric polarization in ferroelectric reaches the saturated polarization, P_s, while electric field is maximum (E_m). The the polarization hysteresis properties versus electric field (P-E) of the ferroelectric $SrBi_2Ta_2O_9$ thin film is plotted in Fig. 6, with saturated polarization P_s = 15 μC/cm^2, remnant polarization P_r = 10 μC/cm^2 and electric field E = 50 kV/cm.

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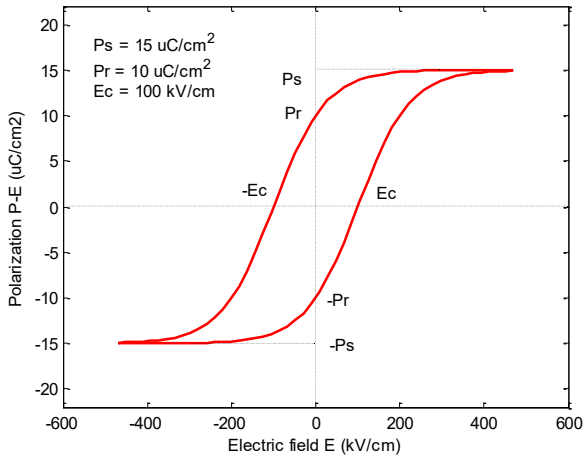

Fig. 6. The saturated polarization hysteresis loop of ferroelectric $SrBi_2Ta_2O_9$

3.2. The $I_{ds} - V_{ds}$ characteristics

As shown in equation (23), the drain-source current (I_{ds}) is dependent on both V_{gs} and V_{ds} that is similar to MOSFET. For the constant V_{gs}, the drain-source current is nonlinear increase when increasing the drain-source voltage. Where V_{ds} is less than V_{TH}, the I_{ds} will increase to exponential function laws. Conversely, where V_{ds} is more than V_{TH}, the I_{ds} will be in constant (saturation state) as shown in Fig. 7.

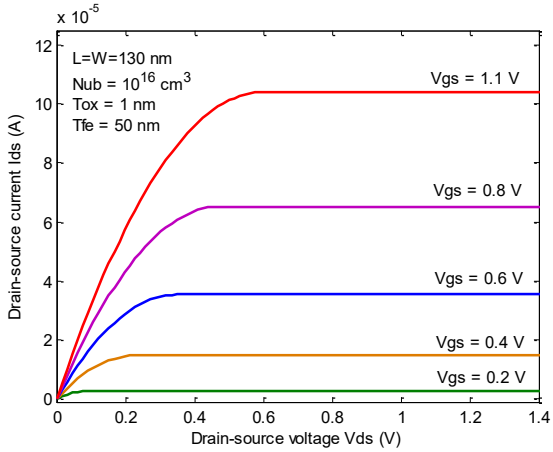

Fig. 7. The Ids - Vgs curves of the FeFET

3.3. Effects of the oxide buffer

In the FeFET, the oxide layer in the gate stack prevents the large number of defects and leakage current from gate to the channel and operates as a buffer with a proper interface with the substrate. Thus, the oxide thickness is strongly affected of the voltage drop over the buffer layer and electric field in the channel. As represented in equation (13), the more oxide thickness increases, the more I_{ds} and memory window decreases. However, in the case of the oxide layer decreases too thin, the leaked current will occur and it can be broken when continuously increasing the gate voltage.

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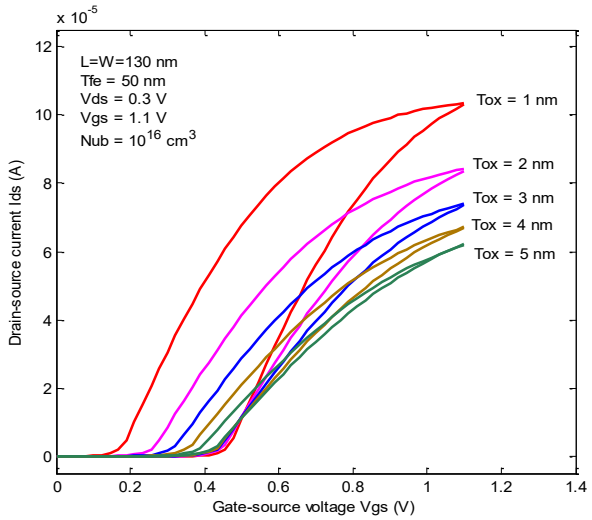

Fig. 8. The Ids - Vgs curves for different thicknesses of oxide insulator

3.4. Ferroelectric capacitor

The ferroelectric layer in the MFIS structure creates a memory function to the ferroelectric capacitor. The ferroelectric capacitance depends on the coercive field created by the gate-source voltage and the thickness of the ferroelectric. Because, the polarization hysteretic of ferroelectric is nonlinear, and ferroelectric capacitance is too. Fig. 9 shown C_{Fe} - V_{gs} characteristic that capacitance is constant value in the accumulation and inversion region. In working region, the more thickness of the ferroelectric increase, the more ferroelectric capacitance decrease.

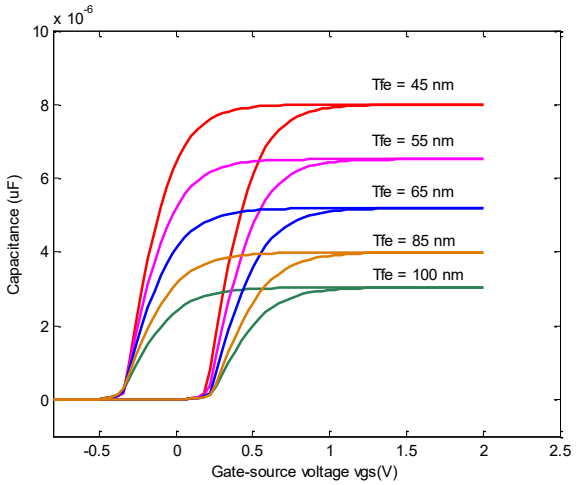

Fig. 9. The $C_{Fe} - V_{gs}$ curves for different thicknesses of ferroelectric $SrBi_2Ta_2O_9$

3.5. Effects of the ferroelectric thickness

The ferroelectric thickness is strong affect to the ferroelectric coercive field in channel. The effect of ferroelectric thicknesses (T_{Fe}) on the drain-source current is similar to the affects of oxide thickness as represented in equation (13). A higher thickness reduces the ferroelectric capacitance and causes a higher voltage drop across the ferroelectric and a smaller across the oxide, the I_{ds} - V_{gs} curve shifts to the right

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and yields a smaller hysteresis and memory window. Thus, the more ferroelectric thickness increases, the more I_{ds} decreases as shown in Fig. 10.

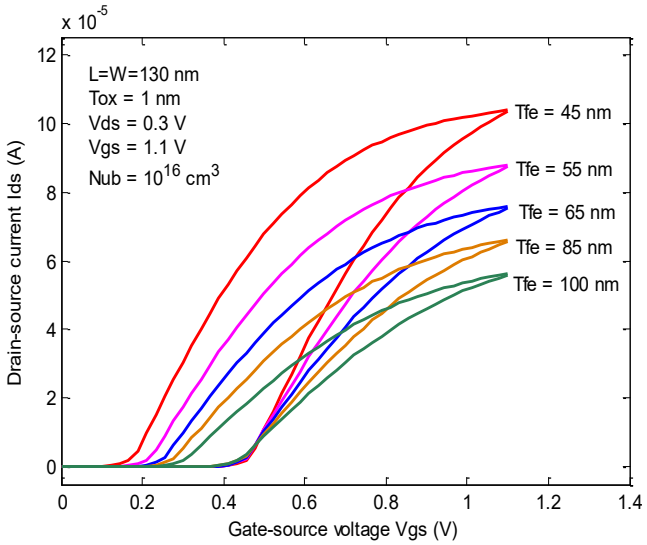

Fig. 10. The I_{ds} - V_{gs} curves for different thicknesses of $SrBi_2Ta_2O_9$;

3.6. The effects of doping concentration

The dependence of silicon doping concentration (N_{sub}) on the I_{ds} is represented in equation (12). It is shown that the doping concentration effects to the conductivity in channel. A higher doping concentration shifts the I_{ds} - V_{gs} curve to the right and yields a smaller memory window. A lower doping yields a larger memory window that expense of lower threshold voltages yields higher leakage current. Thus, the more doping increases, the more I_{ds} and memory window ΔT decrease as represented in Fig. 11.

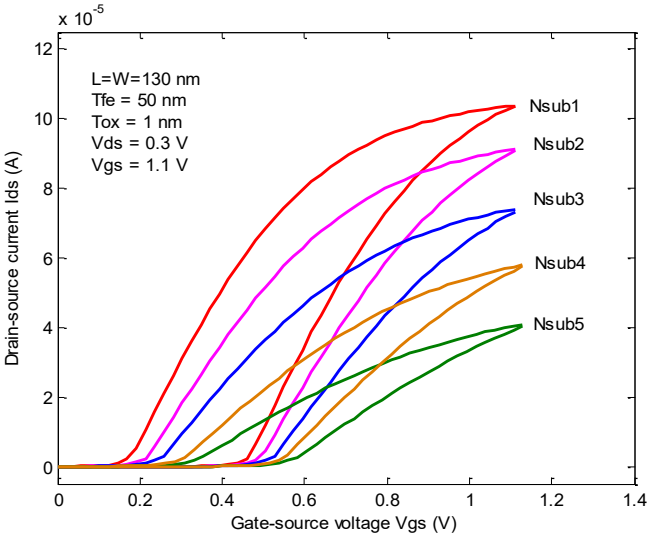

Fig. 11. The I_{ds} - V_{gs} curves for different doping concentration, where $N_1 = 1 \times 10^{16}$ cm^{-3}, $N_2 = 2 \times 10^{16}$ m^{-3}, $N_3 = 3 \times 10^{16}$ cm^{-3}, $N_4 = 4 \times 10^{16}$ cm^{-3}, $N_5 = 5 \times 10^{16}$ cm^{-3}

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3.7. The effects of ferroelectric and oxide thickness ratio

One important parameter that greatly effected to the current-voltage of FeFET is ferroelectric and oxide thickness ratio ($R = T_{Fe}/T_{ox}$). Where the area of the ferroelectric is larger than the area of the oxide that leads to P_r is smaller because the ferroelectric capacitance is larger and the voltage drop across the ferroelectric is smaller. Thus, the more T_{Fe}/T_{ox} increases, the more I_{ds} reduces as shown in Fig. 12. However, the higher ratio can be created a higher dissipation power and it is easily broken when continuous increasing the gate voltage and the memory window is reduced too.

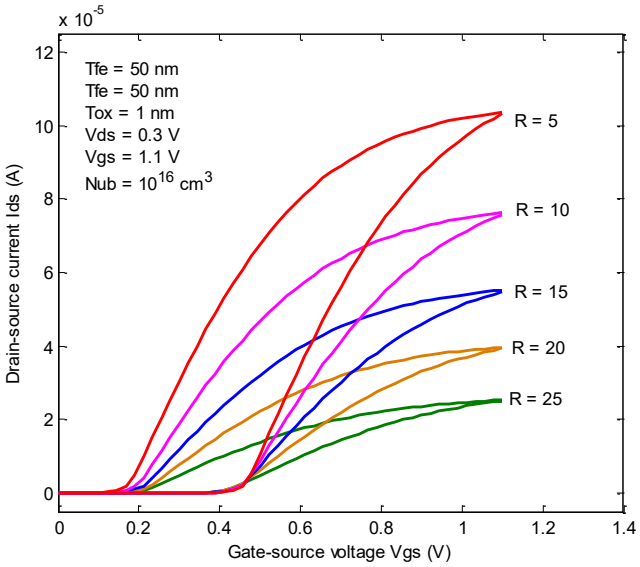

Fig. 12. The I_{ds} - V_{gs} curves different ferroelectric and oxide thickness ratio

4. CONCLUSION

The ferroelectric field effect transistor is offering many advantages compared to other. The effects of $SrBi_2Ta_2O_9$ ferroelectric on current-voltage characteristics of the FeFET was analysed and discussed in this paper. The current-voltage characteristics was calculated under different conditions of device such as adjusting the substrate doping concentration, thickness of oxide and ferroelectric layer, dimensions of the channel, etc. The current-voltage values calculated by this method are almost matching with the results of other methods as presented by Michael Fitsilis [16] and A. Saeidi et al [20], etc. It is shown that the currently analytical method can give out almost accurate results. The note that if reduce the ferroelectric layer with a much smaller area than the oxide layer, the remnant polarization can be increased and the depolarization field can be reduced, this case leads to higher retention times, but it's not a ideal solution to the FeFET processing. Because the oxide layer decreases too thin, the leaked current will occur and it can be broken when continuous increasing the gate voltage. Therefor, the affects of ferroelectric field on the component is an intensive subject to continuous researching.

REFERENCE

[1] Yasuo Tarui, Tadahiko Hirai, Kazuhiro Teramoto, Hiroshi Koike, Kazuhito Nagashima. - Application of the ferroelectric materials to ULSI memories. Appl. Surf. Sci, 113, 656-663, 1997.

[2] Eisuke Tokumitsu, Gen Fujii and Hiroshi Ishiwara. - Electrical properties of metal-ferroelectric-insulator-semiconductor (MFIS)-and metal-ferroelectric-metal-insulator-semiconductor (MFMIS)-FETs using ferroelectric $SrBi_2Ta_2O_9$ film and $SrTa_2O_6$/SiON buffer layer. *Jpn. J. Appl. Phys, 39*, 2125-2130. 2000.

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[3] H. Sugiyama, K. Kodama, T. Nakaiso, M. Noda & M. Okuyama. - Electrical properties of metal-ferroelectric-insulator-semiconductor-FET using $SrBi_2Ta_2O_9$ film prepared at low temperature by pulsed laser deposition. *Integr. Ferroelectr*, *34*, 1521-1531, 2001.

[4] T.P Ma, J.P Han. - Why is nonvolatile ferroelectric memory field-effect transistor still elusive? *IEEE Electron. Device Lett*, *23*, 386-388, 2002.

[5] Eisuke Tokumitsu[1], Kojiro Okamoto[2] and Hiroshi Ishiwara. - Low voltage operation of nonvolatile metal-ferroelectric-metal-insulator-semiconductor (MFMIS)-field-effect-transistors (FETs) using Pt/ $SrBi_2Ta_2O_9$/Pt/$SrTa_2O_6$/SiON/Si structures. *Jpn. J. Appl. Phys*, *40*, 2917-2922, 2001.

[6] S. Sakai, R. Ilangovan. - Metal-ferroelectric-insulator-semiconductor memory FET with long retention and high endurance. *IEEE Electron Device Lett, 25*, 369-371, 2004.

[7] S. Sakai. - Gate Materials and Fabrication-processes of Metal-ferroelectric-insulator-semiconductor Memory FETs with Long Data Retention. *Adv. Sci. Technol*, *45*, 2382-2391, 2006.

[8] Horiuchi, T. Takahashi, M. Li, Q.H. Wang, S.Y. Sakai, S. Lowered operation voltage in Pt/$SrBi_2Ta_2O_9$/HfO_2/Si ferroelectric-gate field-effect transistors by oxynitriding Si. *Semicond. Sci. Techno*, *25*, 055005, 2010

[9] E. Nakamura and T. Mitsui. - Complex Perovskite type Oxides, Landolt and Bornstein, Springer-Verlag, vol.28, 1990.

[10] C. A-paz de Maraujo, j. D. Cuchiaro, l. D. Mcmillan, M. C. Scott and J. F. Scott. - Fatigue-Free Ferroelectric Capacitors with Platinum Electrodes, *Nature*, 374, 627-629, 1995.

[11] Masanori Fukunaga, Masaki Takesada, Akira Onodera. - Ferroelectricity in Layered Ferovskites as a Model of Ultra-Thin Films, World Journal of Condensed Matter Physics, 6, 224-243, 2016.

[12] Haruyasu Yamashita, Keiji Yoshio, Wataru Murata[1] and Akira - Structural Changes and Ferroelectricity in Bi-Layered $SrBi_2Ta_2O_9$, *Japanese Journal of Applied Physics*, 41, 7076, 2002.

[13] T. Kanashima and M. Okuyama, - Analyses of high frequency capacitance-voltage characteristics of metal-ferroelectricinsulator- silicon structures, *Jpn. J. Appl. Phys.*, vol. 38, 2044–2048, 1999.

[14] S.L. Miller and P. J. McWhorter, - Physics of the ferroelectric nonvolatile memory field effect transistor, *Journal of Applied Physics*, 72, 5999, 1992.

[15] Hang-Ting Lue, Chien-Jang Wu et al - Device Modeling of Ferroelectric Memory Field-Effect Transistor for the Application of Ferroelectric Random Access Memory, IEEE *transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 50, no. 1, 2003.

[16] Michael Fitsilis. - Scaling of the Ferroelectric Field Effect Transistor and Programming Concepts for Non-vlatile Memoriey Applications, *doctoral thesis, Universitat der Bundeswehr Hamburg*, 2005.

[17] Y. Tsividis. - Operation and Modeling of the MOS Transistor, *McGraw-Hill*, 1999.

[18] T. Mihara, US Patent 5,515,311, 1996.

[19] Yu, Hyung Suk. - Performance Evaluation and Improvement of Ferroelectric Field-Effect Transistor Memory. UCLA Electronic Theses and Dissertations, 2015.

[20] A. Saeidi , A. Biswas, Adrian M. Ionescu. - Modeling and simulation of low power ferroelectric nonvolatile memory tunnel field effect transistors using silicon-doped hafnium oxide as gate dielectric, *Solid-State*

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Electronics 124, 16–23, 2016.

[21] Cho, Y. *et al*. Enhanced ferroelectric property of p(VDF-TrFE-CTFE) film using room-temperature crystallization for high-performance ferroelectric device applications, *Adv. Electron. Mater. 2*, 1600225, 2016.

[22] Kwok Ng, Steven J. Hillenius, and Alexei Gruverman, - Transient Nature of Negative Capacitance in Ferroelectric Field-Effect Transistors, *Journal reference:Solid State Communications*.265, 12-14, 2017.

PHÂN TÍCH CÁC ẢNH HƯỞNG CỦA ĐIỆN TRƯỜNG SẮT ĐIỆN ĐẾN ĐẶC TÍNH DÒNG ĐIỆN - ĐIỆN THẾ CỦA TRANSISTOR HIỆU ỨNG TRƯỜNG SẮT ĐIỆN SỬ DỤNG MÀNG MỎNG $SRBI_2TA_2O9$

Tóm tắt. Bài viết này trình bày một ý tưởng phân tích mới cho các đặc tính dòng điện - điện thế của transistor hiệu ứng trường sắt điện (FeFET), đây là một linh kiện điện tử tiềm năng để chế tạo các loại bộ nhớ không bay hơi. Trong nghiên cứu này, mô hình FeFET sử dụng màng mỏng Pt / SrBi2Ta2O9 / Insulators / Si như là một khối cổng hiệu ứng đã được đề xuất và đánh giá. Chúng tôi đã nghiên cứu ảnh hưởng của sự phân cực sắt điện đối với các đặc tính dòng điện - điện thế của FeFET dựa trên phương pháp phân tích của linh kiện CMOS, đặc tính trễ phân cực so với trường điện (P-E) của vật liệu sắt điện được phân tích kỹ với hai tham số phân cực bão hòa và không bão hòa. Sau đó, bằng cách phân tích toán học, các giá trị dòng điện - điện thế được tính toán theo các điều kiện khác nhau như sử dụng sự khác biệt của nồng độ pha tạp bán dẫn, độ dày lớp cách điện oxit, độ dày lớp điện sắt, nhiệt độ làm việc ... Cuối cùng, các kết quả đã được mô phỏng bằng phần mềm Matlab, qua đó cho chúng ta cái nhìn tổng quan về các thuộc tính của linh kiện điện tử này.

Từ khoá. *Vật liệu sắt điện, Transistor hiệu ứng trường sắt điện, FeFET, bộ nhớ không bay hơi.*

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